Amendments to the Claims

1-44. (Cancelled)

45. (New) A test circuit that is incorporated in a device, the test circuit being operable to carry out a verification of a first connection node for outputting a signal of said device in a usual operation, said test circuit comprising:

a test data generating circuit operable to generate test data for carrying out said verification; and

a test output buffer connected to said first connection node, the test output buffer being operable to receive test data from said test data generating circuit and to output the test data to said first connection node.

46. (New) The test circuit as claimed in claim 45, further comprising a test input circuit connected to a second connection node to which a signal is applied, said test input circuit being operable to receive test data that are input to said second connection node.

47. (New) The test circuit as claimed in claim 46, wherein said test circuit further comprises a test data processing circuit operable to process said test data.

48. The test circuit as claimed in claim 46, wherein the input signal is a differential signal, the circuit or device further comprising a data input buffer operable to

convert the differential input signal to a single end signal, and to supply the single end signal to an internal circuit.

49. (New) The test circuit as claimed in claim 46, further comprising a test data processing circuit operable to process said test data, said test data processing circuit comprising at least one flip-flop circuit.

50. (New) The test circuit as claimed in claim 45, wherein said test circuit further comprises ESD protectors connected to said first connection node.

51. (New) The test circuit as claimed in claim 45, further comprising a circuit operable to supply said test data to said first connection node based on a test mode signal.

52. (New) The test circuit as claimed in claim 45, wherein said test data are boundary scan register signals.

53. (New) The test circuit as claimed in claim 45, further comprising a data output buffer operable to convert a single end signal from an internal circuit to a differential signal, and to supply the differential signal to said first connection node.

54. (New) The test circuit as claimed in claim 45, wherein a signal line connected to said first connection node is provided with a terminating resistor.

55. (New) The test circuit as claimed in claim 45, wherein said test data generating circuit comprises a circuit that has a register function capable of performing scanning.

56. (New) A semiconductor integrated circuit device having an output circuit operable to transmit a signal via a first connection node, and a test circuit operable to carry out a connection verification of said first connection node in a usual operation, said test circuit comprising:

a test data generating circuit operable to generate test data for carrying out the connection verification of said first connection node; and

a test output buffer connected to said output circuit, the test output buffer being operable to receive test data from said test data generating circuit and to output the test data to said first connection node.

57. (New) The semiconductor integrated circuit device as claimed in claim 56, wherein said output circuit is operable to output a differential signal to said first connection node.

58. (New) The semiconductor integrated circuit device as claimed in claim 57, wherein said test circuit is operable to carry out the connection verification of said first connection node in a differential signal status.

59. (New) The semiconductor integrated circuit device as claimed in claim 56, wherein said test circuit further comprises ESD protectors connected to said first connection node.

60. (New) The semiconductor integrated circuit device as claimed in claim 56, further comprising:

an input circuit operable to receive a signal input via a second connection node; and

a test input buffer, connected to said second connection node, and operable to receive test data input to said second connection node.

61. (New) The semiconductor integrated circuit device as claimed in claim 60, wherein said input circuit is operable to receive a differential signal.

62. (New) The semiconductor integrated circuit device as claimed in claim 60, wherein said test circuit further comprises a test data processing circuit operable to process said test data.

63. (New) The semiconductor integrated circuit device as claimed in claim 56, further operable to carry out a JTAG test of a device in which a single end terminal and a differential terminal coexist.

64. (New) The semiconductor integrated circuit device as claimed in claim 56, further comprising a circuit operable to supply said test data to said first connection node based on a test mode signal.

65. (New) The semiconductor integrated circuit device as claimed in claim 56, wherein said test data are boundary scan register signals.

66. (New) The semiconductor integrated circuit device as claimed in claim 56, further comprising a data output buffer operable to convert a single end signal from an internal circuit to a differential signal, and to supply the differential signal to said first connection node.

67. (New) The semiconductor integrated circuit device as claimed in claim 60, wherein the input signal is a differential signal, the circuit of device further comprising a data input buffer operable to convert the differential input signal to a single end signal, and to supply the single end signal to an internal circuit.

68. (New) The semiconductor integrated circuit device as claimed in claim 60, further comprising a test data processing circuit operable to process said test data, said test data processing circuit comprising at least one flip-flop circuit.

69. (New) The semiconductor integrated circuit device as claimed in claim 56, wherein a signal line connected to said first connection node is provided with a terminating resistor.

70. (New) The semiconductor integrated circuit device as claimed in claim 56, wherein said test data generating circuit comprises a circuit that has a register function capable of performing scanning.

71. (New) A test circuit operable to carry out a verification of a connection node for outputting a signal in a usual operation, comprising:

a test data generating circuit operable to generate single end test data for carrying out said verification; and

a selector circuit, operable to select the single end test data or a signal from an internal circuit based on a test mode signal, the selector circuit being further operable to convert the selected data or signal to a differential signal, and to output the differential signal.

72. (New) A semiconductor integrated circuit device operable to carry out a verification of a connection node for inputting a signal in a usual operation, comprising:

a data input buffer operable to receive data input to said connection node;

a test input buffer, connected to said connection node, operable to receive test data input to said connection node; and

a test data processing circuit operable to process said test data.

73. (New) The semiconductor integrated circuit device as claimed in claim 72, wherein the input signal is a differential signal.

74. (New) The semiconductor integrated circuit device as claimed in claim 72, further comprising ESD protectors connected to said connection node. .

75. (New) The semiconductor integrated circuit device as claimed in claim 72, further comprising:

a converting circuit operable to convert the input differential signal to a single end signal; and

a data processing circuit operable to process the single end signal.

76. (New) The semiconductor integrated circuit device as claimed in claim 72, wherein said test data processing circuit comprises at least one flip-flop circuit.

77. (New) The semiconductor integrated circuit device as claimed in claim 72, further comprising a test data generating circuit comprising a circuit that has a register function capable of performing scanning.